Nuclear Event Protector

AET, Inc.

Synopsis

The objective of this research is to develop the technologies needed to allow innovative, high performance avionics systems, subsystems, and components the capability of successfully achieving early intercept missile defense in current and future interceptors in all hostile environments. The proposed solution to this problem is to provide subsystem-level detection of the special environment and circumvention of potential damage to commercial integrated circuits by the integration of multiple Nuclear Event Protector (NEP) chips into the system. When a special environment is detected, the NEP interrupts power to critical parts of the system. After the event concludes, the system will have survived the event and the NEP allows the power to be restored to the protected integrated circuits and the system can again function normally.

Present and future systems require special threat environment protection that has advanced characteristics from current parts. These new NEPs will have lower power and be capable of sinking much larger currents at faster speeds. This allows not only detection and circumvention, but an added layer of system protection previously unavailable. The development of these new Nuclear Event Protectors is the thrust of this research. In addition, these new NEPs will be fabricated with a modern small geometry process which is presently a trusted mainstream technology.

1 Introduction

Many military missile and communications systems must survive and live through a significant radiation environment to complete its mission. There is significant interest in being able to use Commercial-off-the-Shelf (COTS) integrated circuits in applications where radiation hardened circuits have been traditionally used. This is because COTS integrated circuits are thought to be higher performance, more reliable and significantly cheaper than custom radiation hardened integrated circuits.

There is a thrust to use COTS IC's in all military systems including those that will have the possibility of being exposed to radiation from a nuclear event. However, it is believed that the COTS IC's will not survive this nuclear radiation event causing loss of communication and function of the missile.

2 The Missile Environment

Modern day COTS integrated circuits are normally fabricated using a sub 0.25 micron CMOS technology. To understand the issues associated with using COTS integrated circuits in missile systems we must examine the specific radiation effects that may be encountered. These include neutrons, total dose ionizing radiation, and transient ionizing radiation. Single event effects are usually not significant in the short flights normally associated with missile system application.

Normally, neutron radiation does not affect this technology because it is CMOS, which operates on majority carriers and the reduction of minority carrier lifetime is not important. In addition, the sub 0.25 micron CMOS technology includes very thin gate oxides, which will only slightly be affected by total dose ionizing radiation. Thus, COTS IC's are naturally hardened to a reasonably high level of total dose radiation. Therefore, the most significant issue that exists with COTS IC's in military missile systems is the possible latch-up and burn-out of the IC due to transient ionizing radiation.

Transient ionizing radiation can be deadly to COTS IC's because this radiation produces large quantities of hole-electron pairs and thus large currents in a normally power-on COTS IC. The only effective way to eliminate this problem is to power down the COTS IC while it is exposed to the transient radiation. This power down can be accomplished by using a special device for COTS IC's that is being developed by AET, Inc. called the Advanced Nuclear Event Protector.

3 The Nuclear Event Protector

The purpose of the Nuclear Event Protector (NEP) is to protect commercial chips from transient ionizing radiation. It does this by detecting a nuclear radiation burst at a radiation level that is much too small to harm the commercial chip, and then perform a shut-down operation for the this chip in a time frame that will not allow the chip to latch-up and burn-out. Then, after the nuclear radiation burst is gone, the NEP effectively turns the commercial chip back on.

The AET NEP IC detects transient ionizing radiation by using a silicon PIN diode to convert the radiation to a photocurrent. The amount of photocurrent is proportional to the size of the diode and the amount of the transient ionizing radiation. This photocurrent is amplified by the silicon IC chip that is part of the NEP and this signal is sent to the digital logic portion of the circuit.

The output of the NEP is normally at a high voltage and high impedance. After the radiation event, the output of the NEP drops to a low voltage and low impedance. The delay time between the radiation hitting the PIN diode and the output signal of the NEP is only about 10 nanoseconds. Then after the radiation pulse is gone, the output reverts to a high voltage in a few microseconds. This delay time is programmable.

The application of the AET NEP to the protection of commercial IC's is both straightforward and simple. The application for the protection of COTS devices by the NEP is illustrated in Figure 1.

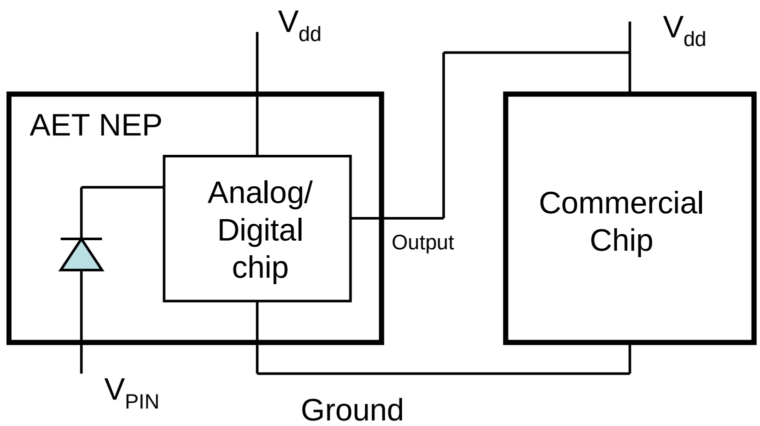

Figure 1. COTS Chip Protection by the AET NEP

Without radiation, the output of the AET NEP is high and the COTS chip functions normally as if the NEP is not there. When a transient ionizing radiation pulse arrives, the output of the NEP switches low (below 0.7 volts) and the COTS chip is effectively debiased. That is, the chip is now biased so that latch-up and permanent damage is not possible. After a programmed time (typically a few microseconds) the radiation pulse has subsided and the NEP output returns to a high voltage. Now, the normal Vdd voltage is restored and the COTS chip can operate normally.

The beauty of this application is that the AET NEP can be added to a system without requiring a new electrical design. A mechanical redesign of the PC board will be needed to include the AET NEP chip(s). The transient ionizing radiation immunity is obtained while keeping the performance and cost effectiveness of the commercial IC chips.

A potential issue with using the AET NEP with commercial chips as shown in Figure 1 is its ability to protect a high speed commercial chip. With very advanced technology, it is probable that the speed of individual gates in the commercial chip will be much faster than the 10 ns delay of the NEP. At first glance, this appears to be a problem and that rapid latch-up and burn-out can occur. However, the fact is that the application shown in Figure 4 will significantly limit the amount of energy that can be expended in the commercial chip during a radiation pulse event. The NEP will switch on and limit the current going into the commercial chip, thus eliminating burn-out. Note that destructive burn-out will not occur even though temporary latch-up can occur.

4 Systems Applications

The real advantage of the AET NEP comes in the systems environment. Figure 2 shows a block diagram of a typical guidance or communication system used on a missile system. Note that the V_{dd} power routing is shown schematically and that the ground is not shown but understood. In Figure 2, six COTS chips are illustrated along with a Voltage Regulator on a PC board. In this configuration, the commercial chips are very vulnerable to transient ionization radiation and system failure can easily happen.

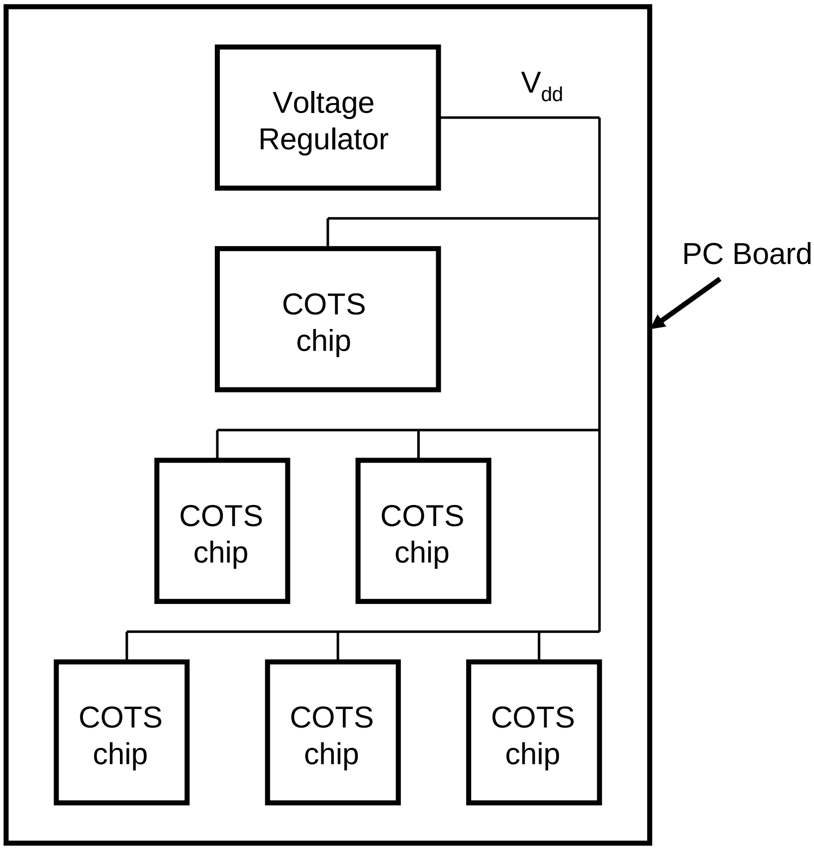

Figure 2. Block Diagram of typical missile system electronics.

To solve the problem of vulnerability to transient ionization radiation, AET proposes to use Nuclear Event Protector chips in conjunction with the commercial electronics. Figure 3 shows a block diagram of the same system as illustrated in Figure 2, with the added Nuclear Event Protectors. In many cases, several NEP's will be utilized to provide the necessary protection as shown in Figure 3.

The NEP circuits are tied to the V_{dd} lines of one or more commercial chips. The number of commercial chips that can be protected by one NEP is dependent on the amount of current that is consumed by each chip and which needs to be shunted by the NEP. In addition, it is assumed that some small resistance will need to be added to each V_{dd} line to act as a current limiter and that an NEP recovery signal will need to be supplied to the Voltage Regulator to reset the V_{dd} voltage.

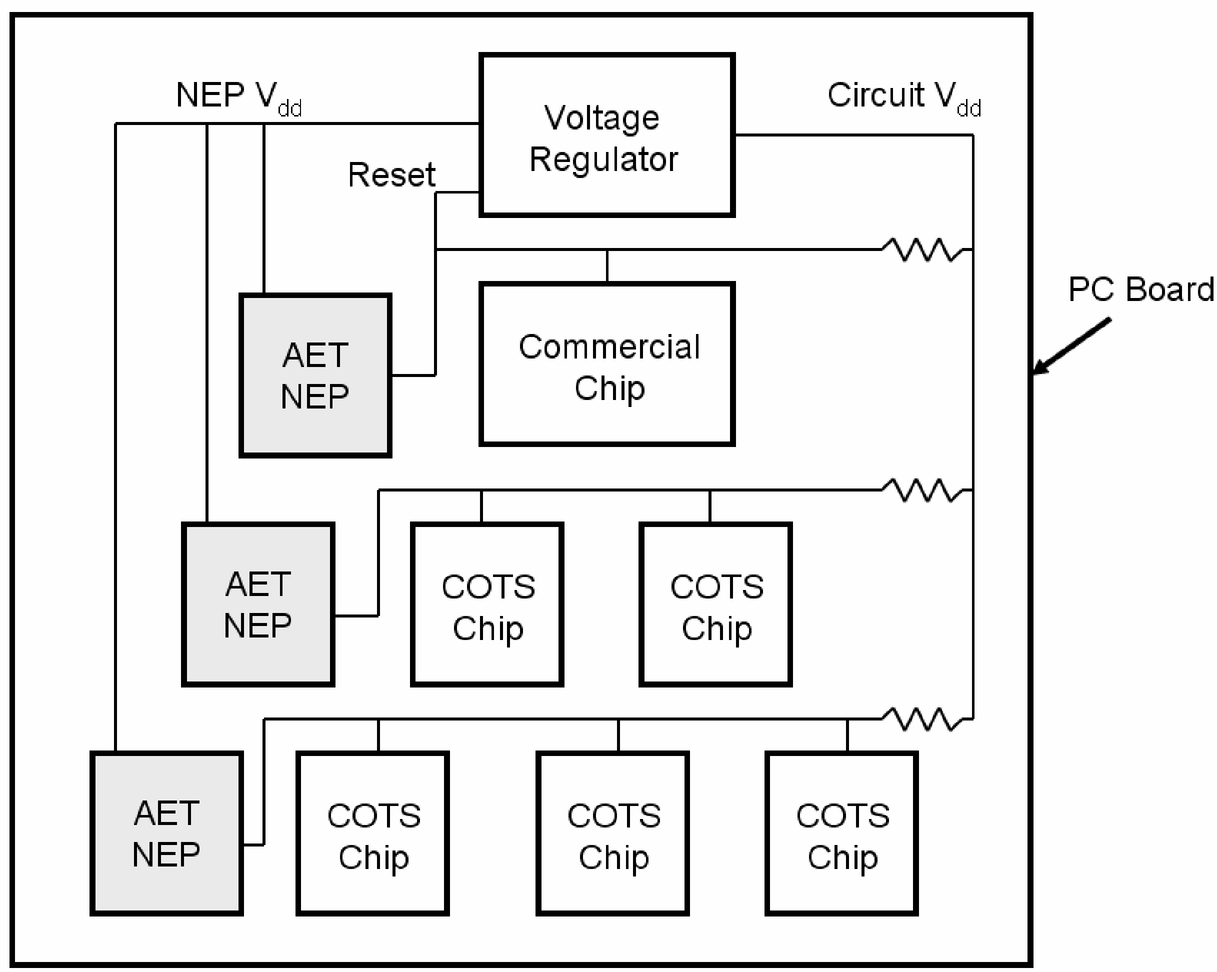

Figure 3. Block Diagram of missile system electronics protected by the AET NEP

A specific application for the AET NEP technology will require significant design verification, but the above proposed concept appears to satisfy much of the requirement to allow commercial chips to withstand environments seen by many missile systems.

5 Analysis of the System Application

The reason this technology will be successful at protecting the commercial IC chips from transient ionizing radiation damage is that AET NEP pulls the V_{dd} line at the commercial chip down to below 0.5 volts in about 10 ns. At this voltage, no latch-up can be sustained in the commercial chip and it is therefore not damaged.

To draw the conclusion that no commercial chip will be damaged in the application in Figure 3, we must analyze several issues involved in the latchup and burnout process. In this analysis, we assume that a transient ionizing radiation pulse strikes the commercial chip with sufficient energy to cause the transistors in the chip to go into a latchup mode.

The actual process that happens in latchup is that parasitic SCR devices in the commercial chip go into an ON condition. At this point, the commercial chip begins to conduct current above its normal rating and if the latchup process is allowed to continue then some metal lines in the chip will eventually burnout. Thus, the chip is destroyed.

To prevent this, the NEP is connected in the system as illustrated in Figure 3. Shortly after the transient ionizing radiation pulse strikes, the output of the NEP switches from a high voltage to a low voltage. The delay time of the NEP is only about 10 ns. If this NEP delay time is faster than the turn-on time of the SCRs in the commercial chip, then the chip never goes into a high current conduction mode and there is no danger to the chip. If the SCR turn-on time is faster than the NEP delay time then the chip can go into a high current conduction mode. It is this second condition that needs analysis as shown below.

It has been well established in the literature that the burnout of interconnect lines in ICs is caused by current generated thermal heating of the metal (see for example "Aluminum Interconnect Response to Electrical Overstress" by J.E. Vinson, *Proceedings of the 24th International Symposium for Testing and Failure Analysis*, 15-19 November 1998, Dallas, Texas). This thermal heating process is relatively slow as compared to electrical delay processes and this allows the NEP to protect the commercial chip.

In this analysis, we considered a number of different silicon CMOS technologies from 1.25 microns down to 0.045 microns (45 nanometers). We calculated the minimum SCR turn-on time for each technology by calculating the bipolar frequency response as a function of the critical geometry of each technology. We estimated burnout time of IC metal lines starting from published data for 1.25 microns technology (see ibid) and scaling this down approximately linearly for smaller technologies. Table 1 shows the results of this analysis.

Table 1

Technology Critical Geometry	Minimum Calculated SRC Turn-on Time	Estimated Metal Burnout Time
1.25 microns	100 nanosecond	32 microsecond
0.70 microns	50 nanosecond	16 microsecond
0.35 microns	13 nanosecond	8 microsecond
180 nanometers	3.4 nanosecond	4 microsecond
90 nanometers	0.8 nanosecond	2 microsecond
45 nanometers	0.2 nanosecond	1 microsecond

The estimated metal burnout time is considered very conservative because all of the data taken on IC metal burnout time is measured with the forcing voltage high compared to actual operating integrated circuit V_{dd}. For example in the reference cited above, the IC metal burnout time is measured for applied voltages between 10 and 20 volts, while the operational V_{dd} is a high of 5 volts for the 1.25 microns technology down to less than 1 volt for the 45 nanometers technology. The lower the operating voltage (or testing voltage) the longer will be the burnout time.

6 Conclusions

The output of the AET Nuclear Event Protector (NEP) transitions from a high voltage to a low voltage in about 10 ns after the incident transient ionizing radiation pulse arrives. Therefore, from Table 1 we see that the technologies with critical dimensions of 1.25 microns down to 0.35 microns are protected because the SCR never turns on and no large current flows in the IC chip.

For technologies with critical dimensions of 180 nanometers down to 45 nanometers, the commercial IC chip may enter into latchup with the resulting high current mode. However, the nuclear event detector will pull the V_{dd} voltage at the chip down to less than 0.5 volts in about 10 nanoseconds and therefore, the chip SCR will have to turn off because there is not enough voltage available to sustain it. Now since the estimated metal burnout time is much larger than the NEP delay time (> 1 microsecond versus 10 nanoseconds), the NEP always protects the IC chip from burnout.

The specific application for the AET NEP technology shown in Figure 3 will require design verification, but the above proposed concept appears to satisfy the requirement to allow commercial IC chips to withstand transient ionizing radiation environments seen by many critical systems.

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